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RECONFIGURABLE NETWORK-ON-CHIP (NoC) ARCHITECTURES FOR EMBEDDED SYSTEMS

Abstract

Communication architectures such as Point-to-Point (P2P) and shared bus are poorly scalable as the number of cores or the communication volume increase. Network-on-Chip (NoC) has been proposed to reduce power consumption and has been widely adopted by the System-on-Chip (SoC) community. Yet, NoCs occupy more area and consume more power as the size of network increases. In this thesis, we propose a novel dynamic reconfigurable P2P (DRP2P) communication architecture for reconfigurable embedded systems, which is an alternative to the conventional NoC architectures. In DRP2P, interconnects are reconfigured on-the-fly as new communication requests arrive at the system. In embedded applications running on the multi-core systems, the traffic flow is usually known. Hence, DRP2P is very suitable for embedded systems. DRP2P is inspired from both P2P interconnects and NoC architecture. If the traffic flow is known in advance, it works as fast as P2P while reconfiguration process is done at the time of computation. Thus, next communication scenario can be established before communication starts. It is as scalable as NoC; increasing the network size, increases reconfigurable wiring area linearly. In order to achieve reconfiguration efficiently, we developed three different dedicated self reconfiguration engines. The latest version of these engines is exploited in DRP2P architecture. DRP2P gives better results than conventional NoCs if the physical placement of cores on the embedded system is done properly by utilizing mapping and routing algorithms. Hence, fast and heuristic mapping and routing algorithms are also designed in the scope of this thesis. Experimental evaluations have shown that DRP2P outperforms conventional NoCs even in the worst case scenario as the amount of data in on-chip communication increases.

PUBLICATIONS

Journals

1- **Salih Bayar** and Arda Yurdakul, "PFROUT: Simultaneous Mapping and Routing on 2-D Mesh Network-on-Chip by Utilizing Particle Filters, " to be submitted.
2- **Salih Bayar** and Arda Yurdakul, "PFMAP: Exploitation of Particle Filters for Network-on-Chip Mapping, " IEEE Transactions on VLSI Systems, Vol. PP, Issue 99, P. 140-159, October 2014
3- **Salih Bayar** and Arda Yurdakul, "An Efficient Self-Reconfiguration Core for Run-time Reconfigurable FPGA Interconnects, " Journal of Systems Architecture, Vol. 58, Issues 3-4, P. 140-159, March 2012

International Conference Papers

1- **Salih Bayar**, Mehmet Tükel and Arda Yurdakul, "A Self-Reconfigurable Platform for General Purpose Image Processing Systems on Low-Cost Spartan-6 FPGAs, " 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip, ReCoSoc'2011, 20-22 June 2011, Montpellier, France.

2- **Salih Bayar** and Arda Yurdakul, "Self-Reconfiguration on Spartan-III FPGAs with Compressed Partial Bitstreams via a Parallel Configuration Access Port (cPCAP) Core, " PRIME 2008 - 4th Conference on Ph.D. Research in Microelectronics and Electronics , 22-25 June 2008, Istanbul, Turkey.
3- **Salih Bayar** and Arda Yurdakul, "Dynamic Partial Self-Reconfiguration on Spartan-III FPGAs via a Parallel Configuration Access Port (PCAP), " HiPEAC Workshop on Reconfigurable Computing, January 27, 2008, Goteborg, Sweden.

National Conference Papers

1- **Salih Bayar** ve Arda Yurdakul, "Gömülü Çoklu İşlemcili Sistemlerde Yeniden Betimlenebilir Haberleşme Protokolleri, " Gömülü Sistemler Sempozyumu, Gömsis 2010, 4-5 Kasım 2010, ITÜ, İstanbul, Türkiye.

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